**CPHE 222: Organization, Architecture, and Assembly Language**

**Homework -- Chapter 5A**

**Exercise 1**: Complete the table below given a direct-mapped cache with 8 rows and a 128-byte block size.

|  |  |  |  |
| --- | --- | --- | --- |
| **Byte address** | **Tag** | **Cache index** | **Block Offset** |
| 0x18AF | 000110 | 001 | 0101111 |
| 0x0211 | 000000 | 100 | 0010001 |
| 0x3033 | 001100 | 000 | 0110011 |
| 0x6215 | 011000 | 100 | 0010101 |

**Exercise 2**: Complete the table below given a direct-mapped cache with 16 rows and a 512-byte block size.

2^4 = 16, 2^9, tag size = 3

|  |  |  |  |
| --- | --- | --- | --- |
| **Byte address** | **Tag** | **Cache index** | **Block Offset** |
| 0x18AF | 000 | 1100 | 010101111 |
| 0x0211 | 000 | 0001 | 000010001 |
| 0x3033 | 001 | 1000 | 000110011 |
| 0x6215 | 011 | 0001 | 000010101 |

**Exercise 3**: Complete the direct-mapped cache diagram below to show its contents at the completion of the following sequence of memory accesses. Also, indicate where each access is a hit, miss, or miss with replace. Assume the block size is 256 bytes and leave the *Data* field blank.

|  |  |  |
| --- | --- | --- |
| **Byte address** | **Type** | **Hit or Miss?** |
| 0x18AF | LW | ❑ Hit ❑ Miss ❑ Miss w/ Replace |
| fa0x0211 | LW | ❑ Hit ❑ Miss ❑ Miss w/ Replace |
| 0x3033 | SW | ❑ Hit ❑ Miss ❑ Miss w/ Replace |
| 0x6215 | LW | ❑ Hit ❑ Miss ❑ Miss w/ Replace |
| 0x021B | SW | ❑ Hit ❑ Miss ❑ Miss w/ Replace |
| 0x181F | LW | ❑ Hit ❑ Miss ❑ Miss w/ Replace |
| 0x0211 | LW | ❑ Hit ❑ Miss ❑ Miss w/ Replace |

**Directed Mapped Cache**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **V** | **D** | **Tag *(write answers in binary)*** | **Data** |
| 00: | 1 |  | 000000 | 0000 |
| 01: | 0 |  | 000110 | 0111 |
| 02: | 0 |  | 0000000 | 1110 |
| 03: | 1 |  | 0110000 | 11011 |